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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,590	03/01/2004	Todd P. Lukanc	H1775	9600

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EXAMINER	
WHITMORE, STACY	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,590	LUKANC ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-20 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-20 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-4, 6-9, 12-18, 20 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over White et al. (US Patent Application Publication 2003/0229868) in view of Hatsch (US Patent 6,735,742).

2. As for the claims White discloses the invention substantially as claimed, including:

Claim 1, White et al. disclose a method of designing an integrated circuit (IC) device having desired electrical characteristics, said method comprising:

providing an initial IC device design (Fig.2, element 36, paragraph [0118]);

generating a layout representation corresponding to the initial IC device design (Fig.2, element 36, paragraph [0118] ; Figs. 10A-10C; paragraph[0144]);

simulating how structures within the layout representation will pattern on a wafer (Figs. 10B-10C; paragraph[0144]);

based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired

electrical characteristics (paragraph[0144]); wherein the desired electrical characteristics include at least one of drive current, gain and switching speed (paragraphs [0006] and [0201]); and

if the actual electrical characteristics associated with the initial IC device design do not sufficiently match the desired electrical characteristics, modifying the initial IC device design (Figs. 10B-10C; paragraphs[0144], [0006], [0014], and [0141]).

Claim 2, White et al. disclose the method of claim 1, wherein the step of determining whether the actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics includes:

determining actual dimensions of structures within the layout representation based on the simulating step (paragraph[0112]-[0114]; [0135]); and

determining the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation (paragraph[0138] and [0144]).

Claim 3, White et al. disclose the method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table (Fig. 25; paragraph [0211]).

Claim 4, White et al. disclose the method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input (paragraphs [0047], [0140], and [0147]).

Claim 6, White et al. disclose the method of claim 1, wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation (paragraph[0009]).

Claim 7, White et al. disclose the method of claim 1, wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design (paragraph[0115]).

Claim 8, White et al. disclose the method of claim 7, further comprising:

determining an amount of process-related variation associated with at

least two structures within the Layout representation of the IC device design (paragraphs[0112]-[0115]).

Claim 9, White et al. disclose the method of claim 8, wherein determining an amount of process-related variation associated with at least two structures within the Layout representation includes:

simulating how structures within the layout representation will pattern on a wafer (paragraphs[0135]-[0138]); and

measuring a feature of the simulated structures, said feature being indicative of process-related variation (paragraphs[0135]-[0138]).

Claim 12, White et al. disclose the method of claim 9, said method further comprising:

measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity (Fig. 3; paragraphs[0120]-[0121] and Fig. 60A; paragraphs[0306]).

Claim 13, White et al. disclose the method of claim 12, wherein the simulated structures are at different locations within the layout representation (Fig. 42; paragraph [0255]).

Claim 14, White et al. disclose the method of claim 9, wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design (Fig. 25; paragraph[0211]; paragraph[0168]), (iii) orientation of a structure, (iv)placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures (Fig. 25; paragraph[0211]).

Claim 15, White et al. disclose the method of claim 9, further comprising: determining whether at least a portion (paragraph[0009]) of the IC device design is optimized with respect to process-related variations (paragraph[0304]).

Claim 16, White et al. disclose the method of claim 15, further comprising:

if a portion of the IC device design is not optimized with respect to process-related variations, modifying at least a portion of the IC device design (paragraphs[0009],[0304], and [0135]) .

Claim 17, White et al. disclose the method of claim 16, wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design (paragraph [0142), (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures (paragraph [0142).

Claim18, White et al. disclose the method of claim 9, wherein the process-related variations include variations caused by at least one of (i) mask generation (pagraph[0112), (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing.

Claim 20, White et al. disclose an integrated circuit (IC) device designed by the method of claim 1 (paragraph [006]).

Claim 31, White et al. disclose a computer-implemented method in which an initial integrated circuit (IC) device design is provided, said method comprising:

generating a layout representation corresponding to the initial IC device design (Fig.2, element 36, paragraph [0118] ; Figs. 10A-10C; paragraph[0144]);

simulating how structures within the Layout representation will pattern on a wafer (Figs. 10B-10C; paragraph[0144]);

based on the simulating step, determining an amount of process-related variation in how at least a portion of the layout representation will pattern on a wafer (paragraph[0009], [0137], and[0144]); and

determining whether the layout representation will pattern as an IC device

having desired electrical characteristics (Fig. 10B, paragraph[0144]); wherein the desired electrical characteristics include at least one of drive current, gain and switching speed (paragraphs[0006] and [0201]).

White does not specifically disclose that desired electrical characteristics include at least one of only gain and switching activity.

Hatsch discloses desired electrical characteristics of at least one of gain and switching activity [col. 2, line 59 – col. 3, line 16; col. col. 14, lines 35-40].

It would have been obvious to one of ordinary skill in the art to combine the teachings of White and Hatsch because adding Hatsch's desired characteristics of gain and/or switching speed would have improved White's system by optimizing layouts for functional capability and desired requirements concerning critical paths which would improve design and circuit performance [see Hatsch, col. 3, especially lines 1-16, and 43-51].

3. Claims 10-11, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over White et al. in view Hatsch (US Patent 6,735,742), and further in view of Rosenbluth et al. (US Patent Application Publication 2002/0140920).

4. As for the claims White in vie of Hatsch discloses the invention substantially as claimed, including:

Claim 10, White in view of Hatsch discloses substantially all the elements in claims 10-11, and 19 as rejected in claims 1, and 7-9 above,
White further discloses Claim 19, the method of claim 11, further comprising:

providing feedback to a designer regarding how a given structure will print on a wafer (White, paragraph [0224]) as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures (White, paragraphs [0115],[0178],[0220] and [0224]).

White in view of Hatsch does not specifically disclose
wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity.
Claim 11, the method of claim 10, wherein:

a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation; and

a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related.

Rosenbluth discloses wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity (paragraphs [0015] and [0019]) and (ii) logarithm of slope of edge intensity (paragraph [0099]);
Claim 11, the method of claim 10, wherein:

a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation (Rosenbluth, paragraphs[0019] and [0082]); and

a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related variation (Rosenbluth, paragraphs[0019]and [0082]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of White in view of Hatsch with the method disclosed by Rosenbluth because such combined method includes slope of edge intensity / logarithm of slope of edge intensity would provide a technique for optimally choosing illumination distribution and mask features (paragraph [0021]).

5. Applicant's arguments with respect to claims 1-4, 6-20, and 31 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
October 17, 2006